CLAIMS

1. An impedance controller that controls termination impedance of at least one output based on a reference value, comprising:

a programmable reference impedance generator that develops a reference impedance controlled by a reference impedance control input;

at least one termination logic element, each including a programmable termination impedance generator coupled to a corresponding output and controlled by termination impedance control input; and

an impedance matching controller that continually adjusts said reference impedance control input to match said reference impedance with the reference value within a predetermined tolerance and that generates said termination impedance control input based on said reference impedance control input.

2. The impedance controller of claim 1, wherein said programmable reference impedance generator and each of said at least one programmable termination impedance generator comprises a binary array of matched P-channel devices.

3. The impedance controller of claim 1, wherein said programmable reference impedance generator and each of said at least one programmable termination impedance generator each provide a pull-up impedance relative to a source voltage.

4. The impedance controller of claim 1, wherein said impedance matching controller comprises:

a voltage sensor that senses a voltage difference between a reference voltage developed across the reference device and a voltage of said programmable reference impedance generator and that asserts an error signal indicative thereof; and

impedance control logic that adjusts said reference impedance control input based on said error signal.

5. The impedance controller of claim 4, wherein the reference value comprises a reference resistor, wherein a voltage source is applied across said reference resistor and said programmable reference impedance generator coupled in series at an intermediate junction, and wherein said voltage sensor asserts said error signal indicative of voltage of said intermediate junction relative to one-half of a voltage level of said voltage source.

6. The impedance controller of claim 4, wherein said impedance control logic receives a clock signal and increments or decrements said reference impedance control input during selected cycles of said clock signal.

7. The impedance controller of claim 1, wherein said impedance matching controller further comprises bias adjustment logic that combines a bias amount with said reference impedance control input to provide said termination impedance control input.

8. The impedance controller of claim 7, further comprising output bias logic that is programmed to provide said bias amount.

9. The impedance controller of claim 8, wherein said output bias logic comprises a plurality of programmable fuses.

10. An integrated circuit (IC), comprising:

a plurality of pins including a reference pin for coupling to an external reference resistor and at least one output pin;

at least one termination logic element, each including a programmable termination impedance generator controlled by a termination impedance control input and coupled to a corresponding one of said at least one output pin; and

impedance matching logic, comprising:

a programmable reference impedance generator controlled by a reference impedance control input;

comparator logic that continually adjusts said reference impedance control input to equalize values of said reference resistor and said programmable reference impedance generator within a predetermined tolerance; and

output termination logic that controls said termination impedance control input based on said reference impedance control input.

11. The IC of claim 10, further comprising:

output bias logic that provides an adjustment value; and

said output termination logic comprising bias adjustment logic that combines said reference impedance control input with said adjustment value to provide said termination impedance control input.

12. The IC of claim 11, wherein said output bias logic comprises a plurality of programmable fuses.

13. The IC of claim 11, wherein said programmable reference impedance generator and each said programmable termination impedance generator comprises a binary array of matched P-channel impedance devices.

14. The IC of claim 10, wherein said comparator logic comprises:

a voltage sensor, coupled to said reference pin and to said programmable reference impedance generator, that detects voltages across said reference resistor and said programmable reference impedance generator and that asserts an error signal indicative thereof; and

impedance control logic that adjusts said reference impedance control input based on said error signal.

15. The IC of claim 14, wherein a reference voltage is applied across said reference resistor and said programmable reference impedance generator coupled in series at a junction and wherein said voltage sensor asserts said error signal indicative of a voltage of said junction within a predetermined error voltage of one-half of said reference voltage.

16. The IC of claim 14, said reference impedance control input comprising a digital value, wherein said impedance control logic receives a clock signal and increments or decrements said reference impedance control input during selected cycles of said clock signal.

17. A method of controlling pull-up termination impedance of at least one output based on a reference resistance, comprising:

applying a reference voltage across the reference resistance and a reference impedance generator coupled in series, the reference impedance generator having a reference impedance input;

periodically adjusting the reference impedance input to equalize voltages of the reference impedance generator and the reference resistance within a predetermined tolerance; and

controlling a termination impedance input of at least one pull-up impedance generator based on the reference impedance input, each pull-up impedance generator coupled to a corresponding output.

18. The method of claim 17, further comprising:

sensing voltage at an intermediate junction of the reference impedance generator and the reference resistance; and

said periodically adjusting comprising comparing the voltage at the intermediate junction with one-half of the reference voltage.

19. The method of claim 17, wherein said periodically adjusting the reference impedance input comprises incrementing or decrementing a digital value during selected cycles of a clock signal.

20. The method of claim 17, further comprising:

programming a bias adjust value; and

said controlling a termination impedance input comprising combining the bias adjust value with the reference impedance input.

21. The method of claim 17, further comprising:

activating selected ones of a binary array of matched P-channel devices of the reference impedance generator based on the reference impedance input; and

activating selected ones of a binary array of matched P-channel devices of each pull-up impedance generator based on the termination impedance input.